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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/299,659	04/27/1999	YUTAKA TERADA	43889-861	3538

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EXAMINER

FAN, CHIEH M

ART UNIT PAPER NUMBER

2634

DATE MAILED: 09/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/299,659

Applicant(s)

TERADA ET AL. *W*

Examiner

Chieh M Fan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 August 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 5/4/2/1 is/are rejected.
- 7) ☒ Claim(s) 3,4 and 5/3/2/1 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 April 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-5) in Paper No. 6 is acknowledged. The cancellation of the non-elected claims 6 and 7 is also acknowledged.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings are objected to because Fig. 4 does not show the power supply voltage supplied by the power supply circuit 52 to the internal circuit 50 as described in the specification (page 9, lines 8-11). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

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Claim Objections

4. Claims 1-5 are objected to because of the following informalities: "the clock signal" in lines 3-4 of claim 1 should be changed to ---a clock signal---, since this limitation has not been mentioned before in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 5/4/2/1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5/4/2/1 recites the limitation "the delay circuit" in lines 1-2. It is not clear whether this delay circuit is referred to the first delay circuit (see line 6 of claim 4) or the second delay circuit (see line 11 of claim 4).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

8. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki (US Patent 5,952,857).

Regarding claim 1, Suzuki discloses an input circuit (Fig. 1, col. 2, lines 66-67, also see col. 3, line 24 through col. 5, line 8) comprising:

delay means (14 in Fig. 1, col. 4, lines 19-28) for defining a delay time ("Ts" at the bottom of Fig. 2F, also see col. 4, lines 25-31) for at least one logical state of a data signal (see the signal "A1" entering the latch 15-1 in Fig. 1, or the signal "B1" entering the latch 15-2 in Fig. 1; the data signals A1 and B1 can also be seen in Figs. 2E and 2F, respectively) and thereby delaying a clock signal (the clock signal output from the DLL circuit 13-1 in Fig. 1) for the delay time defined (col. 4, lines 25-28); and

a holding circuit (15-1 or 15-2 in Fig. 1) for holding the data signal responsive to the delayed clock signal (col. 4, lines 60-65, also see col. 4, lines 25-31).

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Regarding claim 2, Suzuki further teaches that the delay means defines the delay time such that an edge of the clock signal, on which the data signal is intended to be latched and which is included within a transition interval of the data signal (see col. 4, lines 19-25, note that since the clock signal CLK output from the DLL circuit 13-1 is in synchronism with the data signals A1 and B1, the edge of the clock signal CLK output from the DLL circuit 13-1 is therefore included in the transition interval of the data signal A1 or B1; also see Fig. 2A for the clock signal CLK, Fig. 2E for the data signal A1, and Fig. 2F for the data signal B1, note that the raising edge of CLK is within the transition interval of A1 or B1), is delayed to a point in time after the transition interval of the data signal is over (see Figs 2A, 2D, 2E and 2F; as shown in Figs. 2A, 2D, 2E and 2F, the clock signal CLK output from the DLL circuit 13-1 is delayed by a time T_s to produce the delayed clock CLK1, and the raising edge of the delayed clock signal CLK1 is at a point in time after the transition interval of the data signal A1 or B1 is over, also see col. 1, line 66-col. 2, line 3; col. 2, lines 31-36).

Allowable Subject Matter

9. Claims 3, 4 and 5/3/2/1 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and rewritten to overcome the claim objection set forth in Paragraph 4 of this Office Action.

Claim 5/4/2/1 is objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and rewritten to overcome the claim objection and the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in Paragraph 4 and Paragraph 6, respectively, of this Office action.

10. The following is a statement of reasons for the indication of allowable subject matter:

Claims 3 and 5/3/2/1 are allowable over the prior art of record because the prior art of record does not teach or suggest a comparator for comparing the edge of the clock signal, on which the data signal is intended to be latched, to at least one of leading and trailing edges of the data signal.

Claims 4 and 5/4/2/1 are allowable over the prior art of record because the prior art of record does not teach or suggest a comparator for comparing the edge of the clock signal, on which the data signal is intended to be latched, to at least one of leading and trailing edges of the data signal, a first delay circuit for defining the delay time for a logically high state of the data signal based on a result of comparison, and a second delay circuit for defining the delay time for a logically low state of the data signal based on a result of comparison.

Conclusion


11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Saeki (US Patent 6,275,547) teaches a clock recovery circuit comprises a first delay circuit and a second delay circuit and a latch circuit, wherein the latch circuit latches a data signal based on the clock signal extracted from the first and second delay circuits. Akashi (US Patent 6,178,212) discloses a retiming circuit comprises a flip-flop that samples a data signal based on a delayed clock signal, wherein the delay time is controlled by the result of detecting the phase difference between the data signal and a reference clock signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chieh M Fan whose telephone number is (703) 305-0198. The examiner can normally be reached on Monday-Friday 8:00AM-5:30PM, Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (703) 305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.


Chieh M Fan
Examiner
Art Unit 2634

cmf
August 21, 2002